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| EXAMINER | |
|---|---|
| TABONE JR, JOHN J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | 8 |

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/933,468 | MACLELLAN, CHRISTOPHER S | |
| | Examiner | Art Unit | |
| | John J. Tabone, Jr. | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-24 have been examined.

### *Claim Objections*

2. Claim 5 is objected to because of the following informalities: This claim is unclear to the Examiner as to what is being invalidated. Further explanation and appropriate correction is required.

3. Claim 6 is objected to because of the following informalities: This claim is unclear to the Examiner. The claim language does not describe of make clear which of the two control signals may be selected. Further explanation and appropriate correction is required.

4. Claims 9 and 21 are objected to because of the following informalities: This claim is unclear to the Examiner. It is not clear how the second logic section may be used in causing the memory to store an erroneous value. Further explanation and appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 3-6, 9, 10, 13, 21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

On line 7, the sited limitation states: "a third logic section that selectively couples one of the first logic section and the second logic section to the SUT...". A previous disclosure sites a first logic section meaning a single first logic section. Using one of the first logic section implies more than one and therefore renders the claim indefinite. Also, the above stated limitation states that "a third logic circuit that selectively couples...". The word "selectively" implies the "third logic section" couples the first logic section or the second logic section to the SUT not both. This also renders the claim indefinite. For purpose of examination the Examiner will reading this claim as "a third logic section that selectively couples ~~one of~~ the first logic section or the second logic section to the SUT...".

Also, the use of the word "may" on line 17 is non-functional language and, therefore, renders the claim indefinite. The Examiner will examine this claim with "may" removed from the claim language to read "the second logic section transmits...".

Claim 3-5:

The use of the word "may" in these claims is non-functional language and, therefore, renders theses claims indefinite. The Examiner will examine this claim with "may" removed from the claim language to read "the second logic section transmits...".

Claims 6, 9 and 21:

The use of the phase "may be" in this claim is non-functional language and, therefore, renders the claim indefinite. The Examiner will examine this claim with "may" removed from the claim language to read "the second logic section transmits...".

Claim 10:

On lines 7 and 8, the sited limitation states: "and being configured to selectively couple one of the first logic section and the respective second logic section to a respective system-under-test...". A previous disclosure sites a first logic section meaning a single first logic section. Using one of the first logic section implies more than one and therefore renders the claim indefinite. Also, the above stated limitation states that "and being configured to selectively couple ...". The word "selectively" implies the "third logic section" couples the first logic section or the second logic section to the SUT not both. This also renders the claim indefinite. For purpose of examination the Examiner will reading this claim as "and being configured to selectively couple ~~one of~~ the first logic section or the respective second logic section to a respective system-under-test...".

Also, the use of the word "may" on line 17 is non-functional language and, therefore, renders the claim indefinite. The Examiner will examine this claim with "may" removed from the claim language to read "the second logic section transmits...".

Claim 13:

On line 4, the sited limitation states: "selectively coupling, via a third logic section, one of the first logic section and the second logic section to the SUT...". A previous disclosure sites a first logic section meaning a single first logic section. Using

one of the first logic section implies more than one and therefore renders the claim indefinite. Also, the above stated limitation states that "selectively coupling, via a third logic section ...". The word "selectively" implies the "third logic section" couples the first logic section or the second logic section to the SUT not both. This also renders the claim indefinite. For purpose of examination the Examiner will reading this claim as "selectively coupling, via a third logic section, ~~one of~~ the first logic section or the second logic section to the SUT...".

Claim 22:

On lines 6 and 7, the sited limitation states: "configuring each respective third logic section to selectively couple one of the first logic section and the respective second logic section to a respective system-under-test...". A previous disclosure sites a first logic section meaning a single first logic section. Using one of the first logic section implies more than one and therefore renders the claim indefinite. Also, the above stated limitation states that "configuring each respective third logic section to selectively couple ...". The word "selectively" implies the "third logic section" couples the first logic section or the second logic section to the SUT not both. This also renders the claim indefinite. For purpose of examination the Examiner will reading this claim as "configuring each respective third logic section to selectively couple ~~one of~~ the first logic section or the respective second logic section to a respective system-under-test...".

6. Claims 11 and 23 are rejected under 35 U.S.C. 112, second paragraph, for insufficient antecedent basis.

Claims 11 and 23:

These claims recite the limitation "the source" is external to the ASIC. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irrinki et al. (US-5987632), hereinafter Irrinki, in view of Lattimore et al. (US-6021512), hereinafter Lattimore.

Claims 1 and 13:

Irrinki teaches a memory storage device 100 which includes a built-in self test (BIST) unit 120 (first logic section), which cycles memory array 140 (SUT) through various test patterns (test related signals), and a control block 130 (second logic section). Irrinki discloses control block 130 transmits various inputs to memory storage device 140: address 132, write enable 134, and data in signal 136 (other signals during normal mode). (Col. 3, lines 40-44, 59-60, Fig. 1). Irrinki also teaches an address multiplexer 250 (third logic section) that selects between address 132 from the external pins and BIST address 232 (based on BIST select 124) (transmitted from the first logic

section), and conveys an uncorrected address 116 to corrected address multiplexer 252 (third logic section). Irrinki further discloses multiplexer 252 also receives corrected address 114 from BISR unit 110, along with corrected address select 112 as the control signal (one of the control signals that is external to the first, second and third logic sections and the SUT) which outputs the array address 242 to memory array 140 (SUT). (Col. 5, lines 1-10). Irrinki does not explicitly teach that multiplexer 250 and 252 selectively couples the first the BIST unit 120 (first logic section) and control block 130 (second logic section). However, Irrinki does teach the address multiplexer 250 (third logic section) selects between address 132 from the external pins and BIST address 232 (based on BIST select 124) (transmitted from the first logic section). Lattimore teaches a Bus Interface Unit (BIU) 401 which is coupled to an External Address bus and an External Data bus (external pins) and is also coupled to a CPU 404 which in turn is coupled to multiplexer 410, 412, and 414 (plurality of third logic sections) which in turn is coupled to sub-array 416, 418, and 420 (plurality of system-under-test, SUT). (Col. 5, lines 45-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Irrinki's control block 130 (second logic section) to couple Lattimore's Bus Interface Unit (BIU) 401 and CPU 404 to Irrinki's multiplexer 250. The artisan would have been motivated to do so because this would enable Irrinki to exercise control of the signal coming from the external pins during normal mode. The artisan also, would have been motivated to do so because Irrinki would now have the ability to interface to multiple I/O devices. (See Lattimore, Fig. 7)

Claims 10 and 22:

The motivation to modify Irrinki's control block 130 (second logic section) to couple Lattimore's Bus Interface Unit (BIU) 401 and CPU 404 to Irrinki's multiplexer 250 is per the rejection of claims 1 and 13 above. Irrinki does not explicitly teach a plurality of control blocks 130 (plurality of second logic sections). However, Lattimore teaches the Bus Interface Unit (BIU) 401 the CPU 404 (Irrinki's control block 130 (second logic section)) is coupled to multiplexer 410, 412, and 414 (plurality of third logic sections) which in turn is coupled to sub-array 416, 418, and 420 (plurality of systems-under-test, SUT). (Col. 5, lines 45-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Irrinki's control block 130 (second logic section) to couple multiple occurrences of Lattimore's Bus Interface Unit (BIU) 401 and CPU 404 to multiple occurrences of Irrinki's multiplexer 250 and 252 (plurality of control blocks 130 (plurality of second logic sections)). The artisan would have been motivated to do so because this would enable Irrinki to exercise control of the a plurality signal coming from the external pins during normal mode over a plurality of systems-under-test.

Clams 2 and 14:

Irrinki teaches a memory storage device 100 which includes a built-in self test (BIST) unit 120 (first logic section), which cycles memory array 140 (SUT) through various test patterns (test input signals). (Col. 3, lines 40-44).

Claims 3 and 15:

Irrinki teaches data in multiplexer 256 (second logic section) selects between data in signal 136 from the external pins and BIST data in signal 236 (based on BIST

select 124), (indication signal) and conveys array data in bus 246 to memory array 246. (Col. 5, lines 1-10).

Claims 4 and 16:

Lattimore suggests an I/O adapter 718 (I/O controller), which is connected to the sysytem bus, may be a small computer system interface ("SCSI") adapter that communicates with a disk storage device 720. (Col. 11, lines 25-35).

Claims 5 and 17:

Irrinki suggests the CPU 404 receives information (the indication) from the BIU 401 (second logic section) to accesss the memory arrays 416-n+1. (Col. 9, lines 61-64).

Claims 6 and 18:

Irrinki teaches an address multiplexer 250 selects between address 132 from the external pins and BIST address 232 (based on BIST select 124) (assertion of one of the two control signals). (Col. 5, lines 3-6).

Claims 7 and 19:

Irrinki teaches that BIST unit 120 (first logic section) includes a comparator 240 that compares the values on BIST data in signal 236 (expected test outputs) and data out signal 138 (test outputs), asserting error signal 248 if a mismatch is detected (determine the results of the testing).

Claims 8 and 20:

Irrinki teaches that when the BIST select signal 124 and Correct address select signal 112 is asserted (both control signals are asserted) the BIST address 232 (from first logic section) is presented on the memory array 140 (SUT) over array address 242.

Irrinki further suggests that when the BIST select signal 124 is unasserted (one of the control signals unasserted) the normal signals are presented to the memory array 140 (SUT) from the control block 130 multiplexers 250, 254 and 256 (second logic section). (Col. 5, lines 1-19, 50-62).

Claims 9 and 21:

Irrinki teaches a memory storage device 100 which includes a built-in self test (BIST) unit 120 (first logic section), which cycles memory array 140 (SUT comprises a memory) through various test patterns (test related signals), and a control block 130 (second logic section). Irrinki further suggests that when the BIST select signal 124 is unasserted (one of the control signals unasserted) the normal signals are presented to the memory array 140 (SUT) from the control block 130 multiplexers 250, 254 and 256 (second logic section store an erroneous value). (Col. 5, lines 50-62).

Claims 11 and 23:

Irrinki teaches a method for testing digital electronic memory devices (ASIC). Irrinki also teaches signals 132, 134 and 136 are supplied via external pins. (Col. 1, lines 9-11, Col. 5, lines 4-19).

Claims 12 and 24:

Irrinki teaches that BIST unit 110 (first logic section) is simply a state machine that is programmed to cycle through various test patterns. (Col. 5, lines 28-30).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

Guy J. Lamarre
for

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